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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/824,874 | 04/15/2004 | James D. Ballew | 064747.1012 | 7117 |

45507 7590 06/05/2006

BAKER BOTTS LLP
2001 ROSS AVENUE
6TH FLOOR
DALLAS, TX 75201

| EXAMINER | |
|---|---|
| ZALEPA, GEORGE D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/824,874 | BALLEW ET AL. | |
| | Examiner | Art Unit | |
| | George D. Zalepa | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**DETAILED ACTION**

1. Claims 1-27 have been considered by the examiner.

***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Declaration filed on 15 April 2004.

***Information Disclosure Statement***

3. The information disclosure statements (IDS) submitted on 4/15/2005, 8/1/2005, 8/15/2005, 10/10/2005, 3/8/2006, 5/8/2006 has been considered by the examiner.

***Specification***

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Computing system employing multiple nodes capable of communicating to one another via a switch network.

5. The use of the trademark HYPERTRANSPORT™ and INFINIBAND® has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

***Claim Objections***

6. Claims 19-20 are objected to because of the following informalities: Claims 19-20 refer to an X, Y, and Z axis. There is no indication of the relationship of each axis relative to the other, thus rendering the claims indefinite. For example, in an extreme case, all axes could be the same vector.

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-27 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 9 and 21 recite the limitation "eight or more ports", this limitation allows for an infinite number of ports and thus renders the claim indefinite. Furthermore, claims 1, 9, and 21 recite the phrase "High Performance Computing" which renders the claims indefinite as what is considered high performance at one point in time may be substantially different in at another point, thus changing the scope of the claim.

9. Claims 3-4, 11-12 and 23-24 contain the trademark/trade name HYPERTRANSPORT™. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name.

10. Claims 7, 15 and 27 contain the trademark/trade name INFINIBAND®. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods

themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-2, 6-10, 14-15, 21-22 and 26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Osten et al. (US Pat. No. 6,735,660; herein referred to as "Osten".).

13. Regarding **independent claim 1**,

14. Osten discloses *a High Performance Computing (HPC) node comprising: a motherboard* [see Osten, Fig. 1; Examiner's note: It is clear that the system in Fig. 1 is intended to be utilized on one motherboard. It would be extremely uncommon for one of ordinary skill in the art to implement each unit on a separate board as it would require an incredible amount of area to house. Furthermore, since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.]; *a switch comprising eight or more ports* [see Osten, Fig. 1, element 24; Col. 5, lines 13-15; Col. 8, lines 18-21; Examiner's note: A switch in the INFINIBAND® environment would inherently contain much more than eight ports. See enclosed article "Switch Chip Fuels Third-Generation Infiniband"], *the switch integrated on the motherboard* [see Osten, Fig. 1, element 24; Examiner's note: Since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.]; *and at least two processors operable to execute an HPC job* [see Osten, Col. 4,

lines 55-57; Fig. 1, elements 12 et al.], *each processor communicably coupled to the integrated switch and integrated on the motherboard* [see Osten, Fig. 1; Examiner's note: As stated above, it is clear all elements left of element 28 are clearly desired to be implement on the same board, thus, are all coupled to each other via bus lines unnumbered in the figure. Furthermore, since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.].

15. Regarding **claim 2**,

16. Osten discloses *the HPC node of claim 1, each processor coupled to the integrated switch through a Host Channel Adapter (HCA)* [see Osten, Fig. 1, element 22; Col. 8, lines 19-21; Examiner's note: Osten also discloses the use of the Infiniband® architecture, which requires the use of a host channel adapter.].

17. Regarding **claim 6**,

18. Osten discloses *the HPC node of claim 1, the integrated switch operable to communicate I/O messages at a bandwidth substantially similar to power of the processors* [see Osten, Col. 8, lines 19-21; Examiner's note: An Infiniband® switch is capable of having a bandwidth of 120 (raw) / 96 (user) Gbit/s of data (quad data rate), clearly similar to the power of a processor.].

19. Regarding **claim 7**,

20. Osten discloses *the HPC node of claim 1, the integrated switch comprising an Infiniband switch* [see Osten, Col. 8, lines 19-21].

21. Regarding **claim 8**,

22. Osten discloses *the HPC node of claim 1, the integrated switch operable to: communicate a first message from a first of the two or more processors; and communicate a second message from a second of the two or more processors, the first and second message communicated in parallel* [see Osten, Col. 8, lines 19-21; Examiner's note: The Infiniband®

architecture inherently comprises a bi-directional serial bus, thus able to transfer data between processors in parallel.].

23. Regarding **independent claim 9**,

24. Osten discloses *a High Performance Computing (HPC) system comprising a plurality of interconnected HPC nodes* [see Osten, Col. 2, lines 3-8], *each node comprising: a motherboard* [see Osten, Fig. 1; Examiner's note: It is clear that the system in Fig. 1 is intended to be utilized on one motherboard. It would be extremely uncommon for one of ordinary skill in the art to implement each unit on a separate board as it would require an incredible amount of area to house. Furthermore, since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.]; *a switch comprising eight or more ports* [see Osten, Fig. 1, element 24; Col. 5, lines 13-15; Col. 8, lines 18-21; Examiner's note: A switch in the INFINIBAND® environment would inherently contain much more than eight ports. See enclosed article "Switch Chip Fuels Third-Generation Infiniband"], *the switch integrated on the motherboard* [see Osten, Fig. 1, element 24; Examiner's note: Since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.]; *and at least two processors operable to execute an HPC job* [see Osten, Col. 4, lines 55-57; Fig. 1, elements 12 et al.], *each processor communicably coupled to the integrated switch and integrated on the motherboard* [see Osten, Fig. 1; Examiner's note: As stated above, it is clear all elements left of element 28 are clearly desired to be implement on the same board, thus, are all coupled to each other via bus lines unnumbered in the figure. Furthermore, since the components (12, 22 24 etc) are single chips operating together, it would be inherent that they would reside on the same board.].

25. Regarding **claim 10**,

26. Osten discloses *the HPC system of claim 9, the two or more processors on each node coupled to the integrated switch through a Host Channel Adapter (HCA* [see Osten, Fig. 1,

element 22; Col. 8, lines 19-21; Examiner's note: Osten discloses the use of the Infiniband® architecture, which requires the use of a host channel adapter.].

27. Regarding **claim 14**,

28. Osten discloses *the HPC node of claim 9, the integrated switch of each node operable to communicate I/O messages at a bandwidth substantially similar to power of the processors* [see Osten, Col. 8, lines 19-21; Examiner's note: An Infiniband® switch is capable of having a bandwidth of 120 (raw) / 96 (user) Gbit/s of data (quad data rate), clearly similar to the power of a processor.].

29. Regarding **claim 15**,

30. Osten discloses *the HPC system of claim 9, the integrated switch of each node comprising an Infiniband switch* [see Osten, Col. 8, lines 19-21].

31. **Claims 21-22** and **26-27** are rejected as being the method of creating the apparatus in **claims 1-2** and **6-7**.

***Claim Rejections - 35 USC § 103***

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 3, 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten in view of Winkler et al. (US Pat. Appl. Pub. 2004/0024949; herein referred to as "Winkler".).

34. Regarding **claim 3**,

35. Osten discloses the limitations as stated in **claim 2**.

36. Osten does not disclose *the HPC node of Claim 2, each processor further coupled to the integrated switch through a Hyper Transport/PCI bridge.*

37. Winkler discloses *the HPC node of Claim 2, each processor further coupled to the integrated switch through a Hyper Transport/PCI bridge* [see Winkler, Fig. 2, element 200].

38. The advantage of utilizing a HyperTransport™/PCI bridge would have been to allow the processors to communicate with peripheral components. Alone, the HyperTransport™ bus and PCI are not compatible, but still many peripheral components are only compatible with the PCI bus. Thus, by not utilizing a HyperTransport™ to PCI bridge, one would eliminate a large number of peripherals. Furthermore, it would have been known that a system implemented with HyperTransport™ is more flexible and faster and utilizing a HyperTransport™/PCI bridge would allow the benefits of a higher speed processor to be combined with PCI bus based peripherals. This concept would have been well known at the time of invention and furthermore has been utilized by a variety of chip manufacturers including AMD, Transmeta, Apple and HP. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a HyperTransport™/PCI bridge with the goal of allowing a node to communicate with peripherals that utilize PCI busses.

39. Regarding **claim 11**,

40. Osten discloses the limitations as stated in **claim 10**.

41. Osten does not disclose *the HPC node of Claim 10 the two or more processors on each node further coupled to the integrated switch through a Hyper Transport/PCI bridge.*

42. Winkler discloses *the HPC node of Claim 10 the two or more processors on each node further coupled to the integrated switch through a Hyper Transport/PCI bridge* [see Winkler, Fig. 2, element 200].

43. The advantage of utilizing a HyperTransport™/PCI bridge would have been to allow the processors to communicate with peripheral components. Alone, the HyperTransport™ bus and

PCI are not compatible, but still many peripheral components are only compatible with the PCI bus. Thus, by not utilizing a HyperTransport™ to PCI bridge, one would eliminate a large number of peripherals. Furthermore, it would have been known that a system implemented with HyperTransport™ is more flexible and faster and utilizing a HyperTransport™/PCI bridge would allow the benefits of a higher speed processor to be combined with PCI bus based peripherals. This concept would have been well known at the time of invention and furthermore has been utilized by a variety of chip manufacturers including AMD, Transmeta, Apple and HP. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a HyperTransport™/PCI bridge with the goal of allowing a node to communicate with peripherals that utilize PCI busses.

44. **Claim 23** is rejected as being the product of the method performed in **claim 3.**

45. Claims 4, 12, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten in view of Barker et al. (US Pat. Appl. Pub. 2004/0268000; herein referred to as "Barker".).

46. Regarding **claim 4,**

47. Osten discloses the limitations as stated in **independent claim 1**.

48. Osten does not disclose *the processors communicably coupled via a Hyper Transport link*.

49. Barker does disclose *the processors communicably coupled via a Hyper Transport link* [see Barker, Para. 0005, lines 7-9].

50. The advantage of coupling the processors in the invention with HyperTransport™ technology as disclosed by Kunjan would have been to allow the processors to communicate with each other via a high-speed bus, as opposed to slower busses. It would have been common knowledge that a faster processor bus would have increased performance and knowing that the HyperTransport™ bus is faster than a PCI bus or the like. Therefore, it would

have been obvious to one of ordinary skill in the art at the time of invention to replace the bus disclosed by Osten with the faster HyperTransport™ bus for the goal of increasing performance.

51. Regarding **claim 12**,

52. Osten discloses the limitations as stated in **independent claim 9**.

53. Osten does not disclose *the two or more processors on each node communicably coupled via a Hyper Transport link*.

54. Kunjan does disclose *the processors communicably coupled via a Hyper Transport link* [see Kunjan, Para. 0038, lines 7-8].

55. The advantage of coupling the processors in the invention with HyperTransport™ technology as disclosed by Kunjan would have been to allow the processors to communicate with each other via a high-speed bus, as opposed to slower busses. It would have been common knowledge that a faster processor bus would have increased performance and knowing that the HyperTransport™ bus is faster than a PCI bus or the like. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to replace the bus disclosed by Osten with the faster HyperTransport™ bus for the goal of increasing performance.

56. **Claim 24** is rejected as being the method of creating the apparatus in **claim 4**.

57. Claims 5, 13, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten in view of Kunjan et al. (US Pat. Appl. Pub. 2003/0188071; herein referred to as "Kunjan".).

58. Regarding **claim 5**,

59. Osten discloses the limitations as stated in **independent claim 1**.

60. Osten does not disclose *each processor communicably coupled to the integrated switch through a north bridge*.

61. Kunjan does disclose *each processor communicably coupled to the integrated switch through a North Bridge* [see Kunjan, Fig. 1, element 105].

62. The use of a north bridge to couple the processors to the switch would have been obvious to one of ordinary skill in the art, as it has been an industry standard configuration to interface a processor with a front side bus for many years. The purpose of a north bridge is to allow fast communications with certain peripherals external to the CPU. Without a north bridge, the processor would be responsible for the capabilities of the north bridge and would have to sacrifice space on the die for the communications functions. This obviously unwanted, as more space is always desired for computational purposes. Furthermore, the north bridge is substantially faster than the south bridge, as it is closer to the chip, and therefore would be a more appropriate choice for interfacing the external nodes as speed is always of concern. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a north bridge in interfacing multiple nodes via a switch.

63. Regarding **claim 13**,

64. Osten discloses the limitations as stated in **independent claim 9**.

65. Osten does not disclose *each processor communicably coupled to the integrated switch through a north bridge*.

66. Kunjan does disclose *each processor communicably coupled to the integrated switch through a North Bridge* [see Kunjan, Fig. 1, element 105].

67. The use of a north bridge to couple the processors to the switch would have been obvious to one of ordinary skill in the art, as it has been an industry standard configuration to interface a processor with a front side bus for many years. The purpose of a north bridge is to allow fast communications with certain peripherals external to the CPU. Without a north bridge, the processor would be responsible for the capabilities of the north bridge and would have to sacrifice space on the die for the communications functions. This obviously unwanted, as more space is always desired for computational purposes. Furthermore, the north bridge is substantially faster than the south bridge, as it is closer to the chip, and therefore would be a

more appropriate choice for interfacing the external nodes as speed is always of concern. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a north bridge in interfacing multiple nodes via a switch.

68. **Claim 25** is rejected as being the method of creating the apparatus in **claim 5**.

69. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten in view of Pechanek et al. (US Pat. No. 5,682,491; herein referred to as "Pechanek".).

70. Regarding **claim 16**,

71. Osten discloses the limitations as stated in **independent claim 9**.

72. Osten does not disclose *the plurality of HPC nodes arranged in a topology, the topology enabled by the integrated fabric of each node.*

73. Pechanek does disclose *the plurality of HPC nodes arranged in a topology, the topology enabled by the integrated fabric of each node* [see Pechanek, Col. 10, lines 40-42; Col. 12, line 66 to Col. 13, line 4; Examiner's note: In these cites, Pechanek discloses multiple topologies. Furthermore, due to the switches disclosed by Osten, it would have been obvious that the nodes are enabled by the fabric to form the topologies.].

74. The advantage of using a topology would have been to allow for nodes to access other nodes in the most efficient way possible, depending on the application. For example, the use of a hypercube topology has many advantages as opposed to system without a set topology such as, higher bandwidth, regular structure and many program structures able to be mapped with adjacency preserved. These advantages are all desired in every computer system and thus would be desired in the environment disclosed by Osten. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a set topology such as the ones disclosed by Pechanek within the system disclosed by Osten.

75. Regarding **claim 17**,

76. Pechanek also discloses *the topology comprising a hypercube* [see Pechanek, Col. 10, lines 40-42].

77. Regarding **claim 18**,

78. Osten and Pechanek disclose the limitations as stated in **claim 16.**

79. Pechanek also discloses *the topology comprising a folded topology* [see Pechanek, Col. 10, lines 40-42].

80. Regarding **claim 19**,

81. Osten discloses the limitations as stated in **independent claim 9.**

82. Osten does not disclose *a first node of the plurality of nodes interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis, a fourth node of the plurality of nodes along a Z axis, and a fifth node along a diagonal axis.*

83. Pechanek does disclose *a first node of the plurality of nodes interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis, a fourth node of the plurality of nodes along a Z axis, and a fifth node along a diagonal axis* [see Pechanek, Col. 12 line 66 to Col. 13, line 4; Fig. 21-A; Examiner's note: A four dimensional hypercube inherently posseses the configuration as stated in claim 19.].

84. The advantage of using a topology would have been to allow for nodes to access other nodes in the most efficient way possible, depending on the application. The use of a hypercube topology has many advantages as opposed to system without a set topology such as, higher bandwidth, regular structure and many program structures able to be mapped with adjacency preserved. These advantages are all desired in every computer system and thus would be desired in the environment disclosed by Osten. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a set topology such as the ones disclosed by Pechanek within the system disclosed by Osten.

85. Regarding **claim 20**,

86. Osten and Pechanek disclose the limitations as stated in **claim 19**.

87. Pechanek also discloses *the connection between the first node and the fifth node operable to reduce message jumps among the plurality of nodes* [see Pechanek, Col. 1, lines 60-61; Col. 2, lines 19-24; Examiner's note: Pechanek discloses allowing a processing element to control a switch that controls where data is sent to. Thus, in a hypercube disclosed by Pechanek (see rejection of claim 19), since node 1 and node 5 are connected (corners of the two cubes comprising a hypercube) data can flow directly from 1 to 5 instead of another necessarily longer path, thus reducing message jumps.].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Zalepa
Examiner
Art Unit 2183
Randolph 2E74
Phone: (571)272-6754

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100